SESSION 21 – TAPA I

Adaptive Equalizers for Serial Communications

Saturday, June 19, 8:00 a.m.
Chairpersons: C.K. Yang, UCLA
M. Matsui, Toshiba

21.1 — 8:00 a.m.

A Quad Multi-Speed Serializer/Deserializer with Analog Adaptive Equalization, H. Wang,, X. Jiang, D. Tam, F. Cheung, D. Cheung, W. Tong, M. Le, Myles Wakayama, J. Van Engelen, V. Parthasarathy, H. Baumer and A. Buchwald*, Broadcom Corporation, Irvine, CA

A quad multi-speed (1.25/1.5625/2.5/3.125Gb/s) serializer/deserializer implemented in 0.25um CMOS technology is described. It uses a 4x interleaved sample-and-hold receiver architecture. An analog adaptive receiver equalizer and a linear phase detector are used for clock and data recovery. At 3.125Gb/s, the serializer RMS jitter is 2.4ps. The serializer/deserializer runs error free for 2^31-1 PRBS data pattern over various length, up to 40-inches, of FR4 PCB trace.

21.2 — 8:25 a.m.

A 3.125Gbps Timing and Data Recovery Front-end with Adaptive Equalization, M.Q. Le, J. Van Engelen, H. Wang, A. Madisetti, H. Baumer and A. Buchwald*, Broadcome Corporation, Irvine, CA

A 3.125Gbps timing and data recovery front-end is described. Adaptive discrete-time analog forward equalizers implemented in the receiver are used to cancel intersymbol interference. The coefficients in the analog equalizers are continuously adjusted by a digital adaptation loop. To save power, the digital adaptation loop operates at a 32x subsample rate. The timing recovery is 2x oversampled and uses these equalizers in its path for robust performance in the presence of intersymbol interference. A quad 3.125Gbps transceiver core has been fabricated in a standard 0.18μm CMOS process.

21.3 — 8:50 a.m.

Adaptive Equalization and Data Recovery in a Dual-Mode (PAM2/4) Serial Link Transceiver, V. Stojanović, A. Ho, B. Garlepp, F. Chen, J. Wei, E. Alon, C. Werner, J. Zerbe and M.A. Horowitz*, Rambus, Inc., Los Altos, CA, *Stanford University, Stanford, CA

Adaptive equalization using data based update filtering allows continuous updates while minimizing the required sampler front end hardware and reducing the cost of implementation in multi-level signaling schemes. With only minor hardware modifications the 4PAM receiver can be configured as a 2PAM loop-unrolled single-tap DFE receiver. A transceiver chip was fabricated in a 0.13um CMOS process to investigate this dual mode operation and the modifications of the standard adaptive algorithms necessary to operate in high speed link environments.

21.4 — 9:15 a.m.

Common-Mode Backchannel Signaling System for Differential High-speed Links, A. Ho, V. Stojanović, F. Chen, C. Werner, G. Tsang, E. Alon, R. Kollipara, J. Zerbe and M.A. Horowitz*, Rambus, Inc., Altos, CA, *Stanford University, Stanford, CA

Common-mode signaling is used to create a backchannel communication path over the existing pair of wires for a self-contained adaptive differential high-speed link transceiver cell. A transceiver chip was designed in 0.13um CMOS to demonstrate the feasibility of simultaneous differential and common-mode signaling. The measured results indicate that this backchannel achieves reliable communication without noticeable impact on the forward link for bandwidths up to 50MHz and swings of 20-100mV.

21.5 — 9:40 a.m.

Receiver Adaptation and System Characterization of an 8Gbps Source-Sinchronous I/O Link Using On-Die Circuits in 0.13μm CMOS, G. Balamurugan, J. Jaussi*, D. Johnson*, B. Casper*, A. Martin*, J. Kennedy*, R. Mooney* and N. Shanbhag, University of Illinois at Urbana-Champaign, Urbana, IL, *Intel Labs, Hillsboro, OR

This paper describes a 0.13μm CMOS, 8Gbps I/O receiver that uses on-die circuits for receiver adaptation and system characterization. On-die adaptive control is used to tune a 4-tap receive-side analog equalizer, cancel receiver offsets, and determine optimal sampling phase. Adaptive equalization improves data rates by 1.3x-2x over 2”-40” FR4 channels. Noise-margin degradation due to statistical variation in adapted coefficients and offsets is less than 3% of the signal swing. On-die circuits are also used to characterize link performance, channel response, and receiver circuits.

Break 10:05 a.m.